UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,458	06/01/2001	Joshua M. Conner	068354.1439	8446

31625 7590 11/24/2004

BAKER BOTTS L.L.P.
PATENT DEPARTMENT
98 SAN JACINTO BLVD., SUITE 1500
AUSTIN, TX 78701-4039

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,458	CONNER ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel).

3. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action mailed on March 25, 2004.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel), in view of Silverbrook, US Patent 6,315,200.

6. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action mailed on March 25, 2004.

Response to Arguments

7. Applicant's arguments filed August 30, 2004 have been fully considered but they are not persuasive.

8. On pages 7 and 8, Applicant argues in essence:

"In Intel's double-shift instructions, "[b]its shifted out of the source operand fill empty bit position in the destination operand, which also is shifted." This is in contrast with "executing the multi-precision shift instruction on an operation within a multi-word value...and concatenat[ing] the shifted value with bits shifted out of a previous shift operation on the same multi-word value." The double-shift instructions discussed in the cited portion of Intel do not discuss operating on "bits shifted of a previous shift operation," as required by the claim."

However, when a multiple bit position shift occurs, operating on bits shifted of a previous operation necessarily occurs for each bit position shift after the first bit position shift. Therefore, Intel has in fact taught operating on bits shifted of a previous operation (Pages 4-16 and 4-17). Therefore this argument is moot.

9. On page 8, Applicant argues in essence:

"In the cited portion of Intel, "[t]he result is stored back into the destination operand." (Intel page 4-16). This is in contrast with "outputting the result," as required by the claim. Intel's double-shift instructions, "bits [are] shifted out of the source operand [and] fill empty bit positions in the destination operand, which also is shifted." (Intel 4-16). Therefore, the result has not been output, because the result is already in the destination operand."

Applicant is correct that the result is stored back into the destination operand. The result being stored back into the destination operand is equivalent to outputting the result to the destination operand (Intel, Page 4-16). Also see the previous office action, page 3, paragraph 9, section b. Therefore this argument is moot.

10. On pages 8 and 11, Applicant argues in essence:

"The carry flag (CF) cited by the Examiner can store, at most, a single bit (Intel page 4-6). This is in contrast with "storing the bits shifted out the operand during the executing into a carry register." Therefore, the cited portion of Intel does not disclose or suggest the limitations of claim 2.

...

In Intel's double-shift instructions, the Carry Flag (CF) cited by the Examiner can store, at most, a single bit (Intel page 4-6). This is in contrast with "a carry register for storing values shifted out of sections of the barrel shifter," as required by the claim."

However, during each bit position shift a bit is stored into the carry flag. A plurality of bit values are shifted into the carry flag when a bit position shift by a number of more than one occurs (Page 4-16). Therefore, Intel has taught storing the bits shifted out the operand during the executing into a carry register (Pages 4-16 and 4-17, CF) and a carry register for storing values shifted out of section of the barrel shifter (Pages 4-16 and 4-17, CF). Therefore this argument is moot.

11. On pages 10 and 11, Applicant argues in essence:

"Applicants note that in Silverbrook, "the bit formally known as bit 0 does not simply replace RTMP...Instead it is XORed with RTMP..." (column 222, lines 20-23). Applicants note that the XOR and OR logical operations are not equivalent. Therefore, the combination of Silverbrook and Intel does not disclose or suggest all limitations of the claim.

...

In Silverbrook, "the bit formally known as bit 0 does not simply replace RTMP....Instead, it is XORed with RTMP...." (column 222, lines 20-23). The Examiner has not cited any examples of "OR logic for concatenating values stored in the...registers with values in the barrel shifter," as required by the claim. Therefore, the combination of Intel and Silverbrook fails to disclose all limitations of claim 9. Furthermore, Applicants renew their objection to the combination of Intel and Silverbrook, as discussed above."

However, an XOR operation is implemented using "AND" and "OR" gates. Therefore when the bit formally known as bit 0 and RTMP values are XORed together, the values are necessarily Ored. Therefore this argument is moot.

12. On page 10, Applicant argues in essence:

"Applicants further contend that the combination of Intel and Silverbrook is improper. The Examiner has not cited language in either reference or within information commonly known to those skilled in the art that provides the necessary motivation or suggestion to combine these two references. Applicants respectfully submit that one of ordinary skill in the art at the time the invention would not be motivated to combine Intel with Silverbrook."

However, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) nd *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the concatenation step of Intel, include logical OR operation, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24). Therefore this argument is moot.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

14. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100